Please add the following Abstract of the Invention.

Abstract

A method for accelerating a pseudo-random input bit flow (PRBS(T_1)), generated at a first relatively low clock frequency (f1), into an identical output bit flow (PRBS(T_0)) at a second relatively high clock frequency (f0), comprising: collecting the output bit flow; delaying the collected flow by a predetermined value (τ); and combining the delayed flow with the input bit flow.